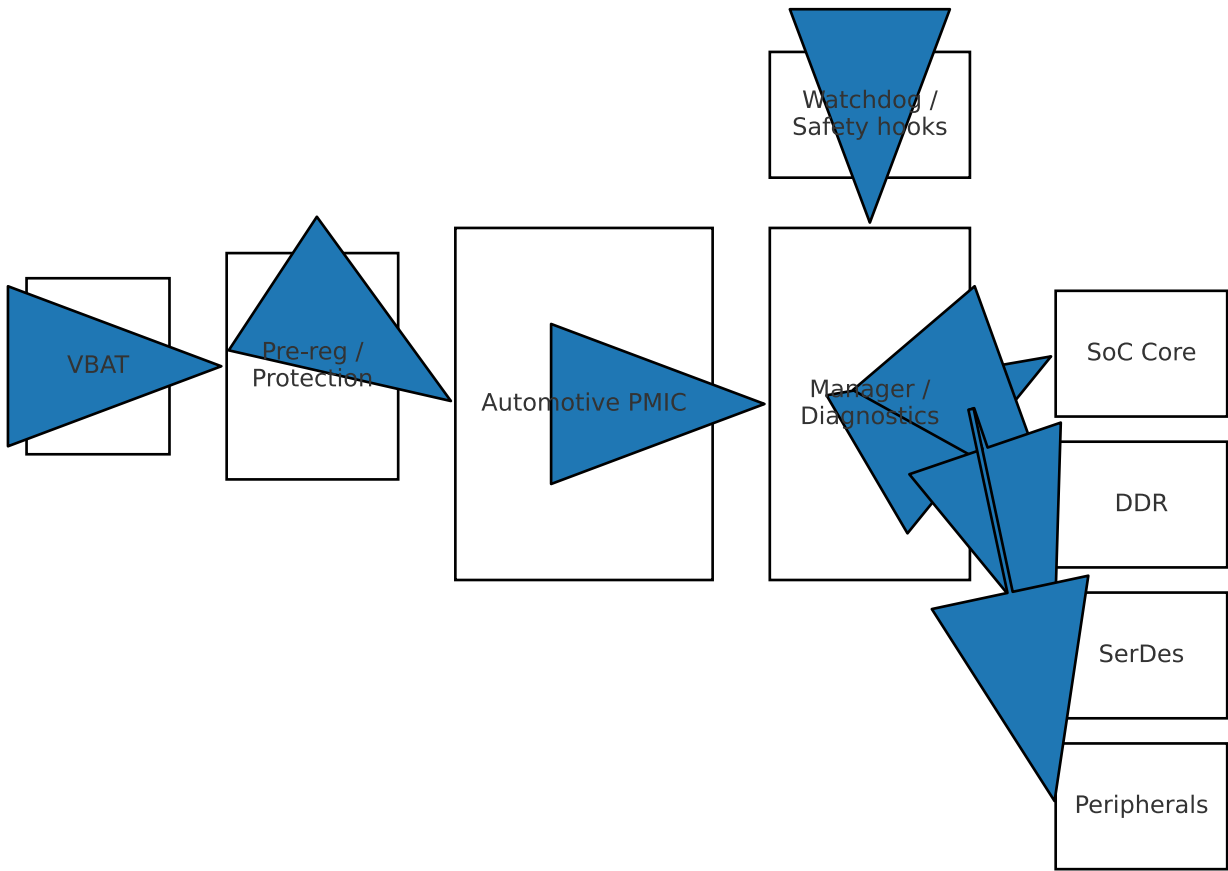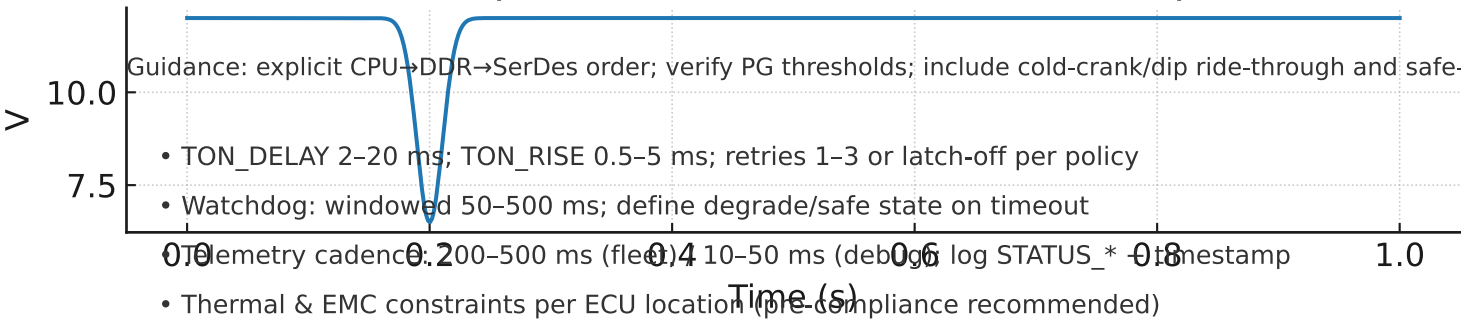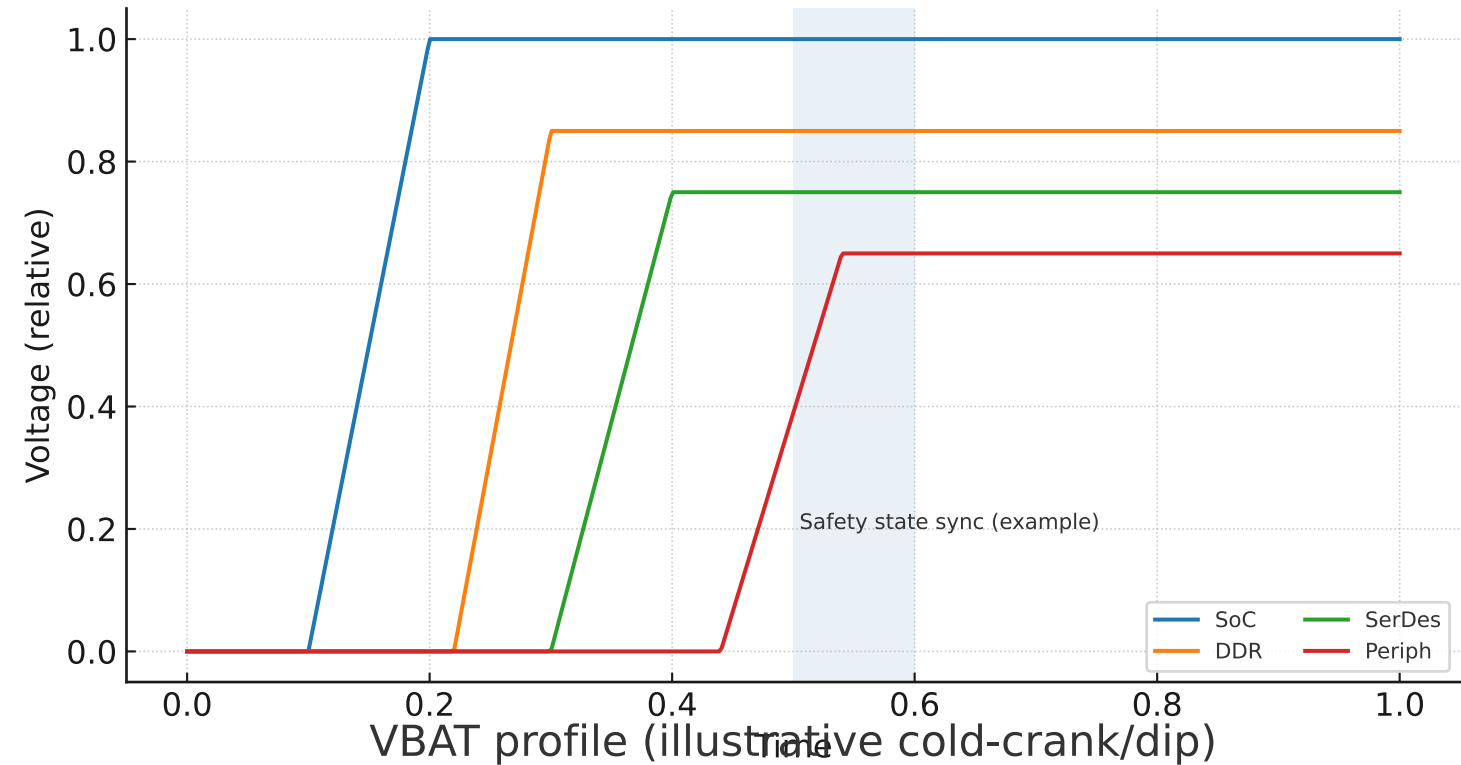# Automotive — Power Management Diagram

VBAT → pre-reg/protection → PMIC + manager → SoC/DDR/SerDes (with safety hooks)

- Automotive PMIC + manager with watchdogs and diagnostics coordinate multi-rail SoC power.
- Fail-safe/operational paths maintain essential domains; sequencing aligns with ASIL goals and safety states.
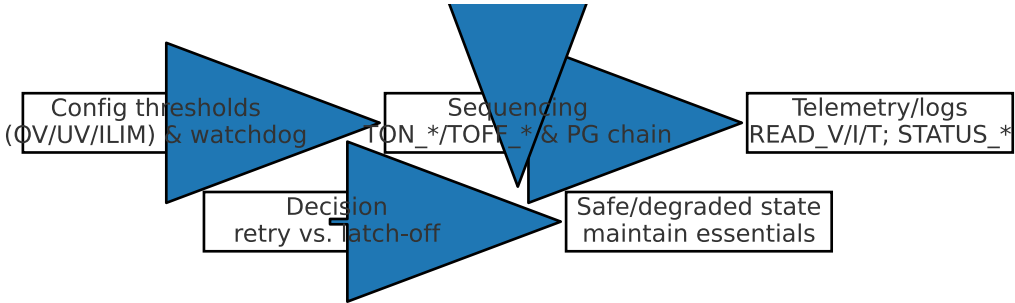
VBAT → pre-reg/protection → PMIC + manager → SoC/DDR/SerDes with safety hooks.

Ordered rails & safety state sync — cold-crank/dip tests included

VBAT profile (illustrative cold-crank/dip)

Guidance: explicit CPU→DDR→SerDes order; verify PG thresholds; include cold-crank/dip ride-through and safe-state handling.

• TON_DELAY 2–20 ms; TON_RISE 0.5–5 ms; retries 1–3 or latch-off per policy

• Watchdog: windowed 50–500 ms; define degrade/safe state on timeout

• Telemetry cadence: 200–500 ms (fleet), 10–50 ms (debug); log STATUS_* + timestamp

• Thermal & EMC constraints per ECU location (pre-compliance recommended)

Configure thresholds/watchdogs → READ_* & status → degrade/safe state on fault

Config thresholds (OV/UV/ILIM) & watchdog	Sequencing TON_*/TOFF_* & PG chain	Telemetry/logs READ_V/I/T; STATUS_*
Decision retry vs. latch-off	Safe/degraded state maintain essentials	

AEC-Q100 Test Flow (brief)

- Grades: 0 / 1 / 2 / 3 by temperature range

- Core items: ESD (HBM/CDM), latch-up, HTOL, temp cycling, THB/HAST, solderability, mechanical shock/vibration

- Board-level: ISO 7637-2 transients, cold-crank/dip, load dump, EMC pre-compliance

Compliance: AEC-Q100, ISO 26262, EMC pre-compliance