ASIC Cost vs Volume Cheatsheet

Quick reference for back-of-envelope planning. Use with the Cost & Volume section to sanity-check assumptions.

Cost Model

Total Cost = **NRE** + (**Unit Cost** × **Volume**) – **BoM savings**

NRE includes: design/verification, masks, packaging NRE, ATE bring-up, engineering samples.

Unit Cost drivers: node, die area, yield, package, assemble, test time, quality targets.

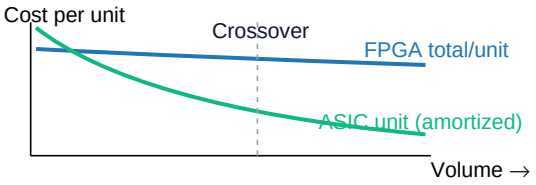
BoM savings: fewer external ICs, smaller PCB/enclosure, simpler assembly.

Three-Volume Scenarios (illustrative ranges only)

Scenario	Volume	Assume Unit Cost*	Est. NRE	Notes
Low	≤ 10k	$X_high	$NRE_low	FPGA or MPW often favorable
Medium	10k–200k	$X_mid	$NRE_med	Crossover range appears
High	≥ 200k	$X_low	$NRE_high	ASIC wins strongly on unit price

* Replace with your node, die, package and test assumptions.

Cost-per-Unit vs Volume (schematic crossover)



MPW Tip

Validate silicon at a fraction of full-mask NRE. Prefer mature nodes, plan package & ATE early, and lock interfaces/power targets before committing to production.

Use this sheet with the Cost & Volume section. For an indicative 48h range, share application, volume tier, node/package, reusable IP, and test constraints.