ASIC Design Flow Checklist

Companion worksheet for Requirements → RTL → Simulation → P&R; → Verification → Tape■Out. Use to track inputs, outputs and sign■offs.

Project / Part:		Target Node:		Package:	
Owner:		Rev:		Date:	

1) Requirements	Owner	Due
■ Freeze spec and KPIs (PPA targets, latency, die size budget)		
■ Partition data path / control / I/O / clock / power domains		
■ Define interfaces & pinout candidates; draft register map (CSR)		
■ Draft verification plan & coverage targets		
■ Compliance: safety / EMC / temperature / lifetime		
Expected outputs		
■ Spec v1.0 & interface doc		
■ Test plan (draft) & acceptance criteria		
■ Risk register & schedule baseline		
Key risks & mitigations		
■ Scope drift; ambiguous requirements		
■ Unrealistic targets vs node/package constraints		

2) RTL	Owner	Due
■ Create synthesizable Verilog/VHDL/SystemVerilog		
■ Clock/reset/CDC strategy documented		
■ Instantiate reusable IP (memories, interfaces, CPU if any)		
■ DFT/scan strategy planned; CSR map frozen		
■ Lint clean; CDC clean (waivers documented)		
Expected outputs		
■ RTL drop + constraints (SDC)		
■ Register map & programming model		
Key risks & mitigations		
■ FPGA-only primitives; non-synthesizable constructs		
■ Timing-unfriendly coding styles		

3) Simulation / Verification (RTL)	Owner	Due
■ Unit & integration testbenches (UVM or equivalent)		

■ Functional & code coverage targets met		
■ Formal checks (as applicable)		
■ Bug list tracked; ECO plan ready		
Expected outputs		
■ Coverage report & sign-off criteria met		
Key risks & mitigations		
■ Coverage holes / missing corner cases		

4) Physical Implementation (Synthesis, Place & Route, STA)	Owner	Due
■ Synthesize netlist with constraints; QoR tracked		
■ Floorplan & power intent (UPF/CPF) finalized		
■ Place/route complete; congestion acceptable		
■ Static timing analysis (all corners/modes) clean		
■ IR/EM & signal integrity checks within limits		
Expected outputs		
■ Timing/power/area reports		
■ GDSII candidate & sign-off checklist		
Key risks & mitigations		
■ Timing closure issues; routing congestion		
■ IR drop & electromigration violations		

5) Sign-off Verification	Owner	Due
■ DRC & LVS clean (Calibre or equivalent)		
■ Gate-level simulation for critical paths & resets		
■ DFT/scan/BIST coverage met; patterns generated		
■ Power/thermal analysis complete		
Expected outputs		
■ Sign-off report bundle		
■ Mask data prepared		
Key risks & mitigations		
■ Late DRC/LVS surprises; insufficient test coverage		

6) Tape-Out & Bring-up	Owner	Due

■ Fab order placed; masks reviewed		
■ Package selected; pinout & PCB constraints locked		
■ ATE program & sockets ready; bring-up plan defined		
■ Firmware & lab scripts prepared		
Expected outputs		
■ Silicon samples & ATE results		
■ Datasheet rev A / Errata list		
Key risks & mitigations		
■ Supply lead-time; respin cost and schedule		

MPW Readiness (optional for small-batch)

Use a multi-project wafer to validate silicon at reduced NRE. Prefer mature nodes, lock interfaces early, plan DFT/ATE and package in parallel.

Tip: Keep this checklist alongside your Gantt or kanban board; convert each unchecked item into a task with an owner and due date.